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(54) **Vertical transistor capacitor memory cell structure and fabrication method therefor.**

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US-A- 4 651 184

IEEE ELECTRON DEVICE LETTERS, vol. EDL-7, no. 2, February 1986, pages 119-121, IEEE, New York, NY, US; H. SHICHIJO et al.: "Trench transistor DRAM cell"

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For simplicity, this cell structure is called a U-SPT cell. Arrangement of the vertical access transistor 10 and the trench storage capacitor 22 as shown in Fig. 1 are different from those of the conventional planar and trench DRAM cells described by H. Sunami in the publication "Cell structures for future DRAM's", IEDM Tech. Dig., pp. 694-697, 1985 and by W. F. Richardson et al, in the publication "A trench transistor cross-point DRAM cell", IEDM Tech. Dig., pp. 714-717, 1985 because it will give the advantages of ultra small size, high packing density, lower soft error rate, less leakage and punch-through currents and better noise immunity.

The new cell is fabricated successfully by using a new self-alignment epitaxial growth method in combination with state-of-the-art CMOS technologies. Two epitaxial layers are grown with an intervening oxide etching step over a substrate wafer already provided with trench storage capacitors. The first and second epitaxial layers simultaneously grow vertically on the bare silicon surrounding the buried storage capacitor and laterally over the oxide. The trench transistor is fabricated in the epitaxial layers.

Fig. 1 illustrates a cross-sectional view of a U-SPT cell fabricated using the method of the present invention illustrated in Figs. 3 through 10, with a top view shown in Fig. 2. The structure of the device of Fig. 1 includes a silicon substrate 16 which, for the purposes of explanation, is p+ type. A p-channel transfer device with gate 48, source 44, and drain 40 is made in an n-well region 36 within a p-type epitaxial layer 14. A trench capacitor is located in substrate 16 and filled with heavily doped p+ polysilicon 26. A composite film 24 of $SiO_2/Si_3N_4/SiO_2$ on the trench sidewalls is provided for the capacitor storage insulator. A p+ doped vertical connection 34 is formed to connect the source region of the transfer device and the storage electrode 26 of the trench capacitor. An interconnection diffusion line 40 used for the bitline is connected to the drain region of the transfer device.

The method steps of the present invention for fabricating the U-SPT structure of Fig. 1 are described as follows:

Step 1) A p- doped monocrystalline silicon film 14 is grown epitaxially on p+ doped substrate 16. A composite layer 12 of SiO_2 20 and Si_3N_4 18 is formed on epitaxial layer 14. After suitable lithography steps, an opening is made in composite layer 12. The composite layer 12 which remains is then used to mask the etch of a trench 12 into substrate 16 by RIE (reactive ion etching) as shown in Fig. 3.

Step 2) After a thin SiO_2 layer is thermally grown on the trench surface, a thin Si_3N_4 layer is deposited and thermally densified in an oxidizing ambient to form composite film 24 for the capacitor storage insulator. A thick, p+ doped polysilicon layer 26 is then deposited to fill the trench as shown in Fig. 3.

Step 3) The polysilicon film 26 is planarized by RIE and/or chemical-mechanical polishing such that the surface of polysilicon 26 is coplanar with the top of substrate 14 as shown in Fig. 3. The nitride/oxide layer 12 over the substrate surface is used for etch stop.

Step 4) An SiO_2 layer 28 is thermally grown on polysilicon 26. The presence of composite film 12 on the monocrystalline regions prevents oxidation of epitaxial layer 14 as shown in Fig. 3. The thickness of SiO_2 layer 28 is much greater than that of the SiO_2 portion 20 of composite layer 12.

Step 5) The Si_3N_4 portion 18 of composite layer 12 is removed by selective isotropic etching. The SiO_2 portion 20 of composite layer 12 is then entirely removed, leaving a thickness of SiO_2 layer 28 on polysilicon 26 by virtue of its much greater thickness compared to the SiO_2 portion 18 of composite layer 12.

Step 6) A monocrystalline, p-type doped layer 30 is grown epitaxially on the exposed surface of epitaxial layer 14 as shown in Fig. 4. Epitaxial layer 30 grows laterally over SiO_2 layer 28 at approximately the same rate as it grows vertically from epitaxial layer 14. In this way, the growth of epitaxial layer 30 is controlled to produce a lateral "window" 50 between its advancing edges over SiO_2 layer 28, illustrated by cross section views.

Step 7) The "window" 50 in epitaxial layer 30 is used as a self-aligned mask for removing SiO_2 layer 28 over polysilicon 26 in window area 50 by either wet chemical, dry plasma or reactive ion etching, as shown in Fig. 5. Thus, a contact region to the trench fill polysilicon 26 is established by a self-aligned epitaxial growth technique rather than by lithographic masking steps.

Step 8) After opening the contact region, another epitaxial layer 32 is grown to fill window 50 as shown in Fig. 6. Note that during this growth a pyramidal region 34 of polycrystalline silicon called "neck" results in the window 50 area of polysilicon trench fill 26. Dopant diffusion from polysilicon trench fill 26 into the polycrystalline region of epitaxial layer 34 during this step and subsequent heat treatments forms a conductive region between the polysilicon trench fill 26 and the wafer surface.

At this point, n-well region, isolation region and p-channel vertical FET device regions are then fabricated in combination with state-of-the-art CMOS and trench technologies to produce

taxial layer (14) and substrate (16) structure;
said polysilicon trench (26) having a silicon dioxide layer (28) thereon, comprising the steps of:

Step 1) form a second epitaxial layer (30) over the first epitaxial (14) and silicon dioxide (28) surfaces of said structure, employing a controlled horizontal epitaxial growth to leave an opening (50) in said second epitaxial layer (30) over said silicon dioxide covered deep trench (26);
Step 2) etch to remove said uncovered silicon dioxide layer (28) over said polysilicon filled trench (26) in said opening (50) in said second epitaxial layer (30) over said deep trench (26), said second epitaxial layer (30) functioning as an etch mask;
Step 3) form a third epitaxial polysilicon layer (32) over said structure, said third polysilicon layer (32) filling said opening (50) in said second epitaxial layer (30), said third epitaxial layer (32) growth causing an epitaxial polysilicon neck (34) to form vertically above said polysilicon filled deep trench (26), and wherein diffusion from said polysilicon neck (34) into said surrounding epitaxial material of said second epitaxial layer (30) forms a source junction;
Step 4) define and etch a shallow trench (42) in said epitaxial layers over said deep trench region (26), said shallow trench (42) extending down and cutting into a portion of said epitaxial polysilicon neck (34);
Step 5) grow a thin layer of oxide (46) on the walls of said shallow trench (42);
Step 6) fill said shallow trench (42) with polysilicon material (48) to form transfer gate and wordline regions for said memory cell.

2. A process for fabricating a semiconductor memory cell structure of the type set forth in Claim 1 wherein step 1 includes the following steps:

Step 1A) on a semiconductor wafer including a first semiconductor type substrate (16) with a second semiconductor type first epitaxial layer (14) thereon, form a nitride layer (18) and oxide layer (20) over said epitaxial layer (14), wherein said nitride and oxide layers are formed having an opening therein to define a storage capacitor region;
Step 1B) using said opening in said oxide and nitride layers (18, 20) as an etch mask, etch a deep trench in said epitaxial layer (14) and substrate (16) structure;
Step 1C) form a composite oxide-nitride layer (24) over the vertical and horizontal surfaces of said trench to provide a storage capacitor insulator;
Step 1D) fill said trench with first semiconductor type polysilicon (26) and form a silicon dioxide layer (28) over the polysilicon top surface of said filled trench (26);
Step 1E) form a second epitaxial layer (30) over the first epitaxial and silicon dioxide surfaces of said structure, employing a controlled horizontal epitaxial growth to leave an opening (50) in said second epitaxial layer (30) over said silicon dioxide (28) covered deep trench (26).

3. A process for fabricating a semiconductor memory cell structure of the type set forth in Claim 1 wherein step 3 further includes the following steps:

Step 3A) define and implant an n-well region in said third epitaxial layer (32);
Step 3B) form a diffusion region (40) in said third epitaxial layer (32) over said deep trench region (26) to form a drain junction region for said memory cell.

4. A process for fabricating a semiconductor vertical access transistor-storage capacitor memory cell structure according to Claims 1 to 3 wherein
said semiconductor substrate (16) is composed of p+ type semiconductor material,
said epitaxial layers (14, 30, 32) are comprised of p- type semiconductor material,
said polysilicon in said deep trench (26) and said epitaxial polysilicon neck (34) are composed of p+ type semiconductor material, and
said polysilicon material (48) in said shallow trench is composed of n+ type semiconductor material.

5. A process for fabricating a semiconductor vertical access transistor-storage capacitor memory cell structure according to Claims 1 to 3 wherein
said semiconductor substrate (16) is composed of p+ type semiconductor material,
said epitaxial layers (14, 30, 32) are comprised of p- type semiconductor material,
said polysilicon in said deep trench (26) and said epitaxial polysilicon neck (34) are composed of p+ type semiconductor material, and
said polysilicon material (48) in said shallow trench is composed of p+ type semiconductor material.

6. A semiconductor memory cell structure of the type including a vertical access transistor self-aligned over a trench storage capacitor

nung aufgebaut werden, um den Bereich einer Speicherkapazität festzulegen;
Schritt 1B) Verwendung der Öffnung in den Oxid- und Nitridschichten (20, 18) als Ätzmaske für die Ätzung eines tiefen Grabens in die Struktur aus Epitaxieschicht (14) und Substrat (16);
Schritt 1C) Bildung einer zusammengesetzten Oxid/Nitridschicht (24) über den vertikalen und horizontalen Oberflächen des Grabens zur Herstellung einer Isolation für die Speicherkapazität;
Schritt 1D) Füllung des Grabens mit Polysilicium (26) des ersten Halbleitertyps und Bildung einer Siliciumdioxidschicht (28) über der Polysiliciumoberfläche des aufgefüllten Grabens (26);
Schritt 1E) Bildung einer zweiten epitaxialen Schicht (30) über den Oberflächen von erster Epitaxie und Siliciumdioxid dieser Struktur unter Verwendung eines gesteuerten horizontalen epitaxialen Wachstums, um eine Öffnung (50) in der zweiten Epitaxieschicht (30) über dem mit Siliciumdioxid bedeckten tiefen Graben (26) zu belassen.

3. Herstellungsverfahren für eine Halbleiter-SpeicherzellenStruktur der in Anspruch 1 dargelegten Art, worin Schritt 3 ferner folgende Schritte einschließt:
Schritt 3A) Festlegung und Implantation eines Bereiches einer n-Wanne in der dritten Epitaxieschicht (32);
Schritt 3B) Bildung eines Diffusionsbereiches (40) in der dritten Epitaxieschicht (32) über dem Bereich des tiefen Grabens (26) zur Erzeugung eines Drain-Überganges für diese Speicherzelle.

4. Hersteilungsverfahren für eine vertikale Transistor-/Kapazitätspeicherzellen-Halbleiterstruktur nach Anspruch 1 bis 3, wobei
das Halbleitersubstrat (16) aus p^+-Halbleitermaterial besteht,
die Epitaxieschichten (14, 30, 32) aus p^--Halbleitermaterial bestehen,
das Polysilicium in dem tiefen Graben (26) und der epitaxiale Polysiliciumhals (34) aus p^+-Halbleitermaterial bestehen,
das Polysiliciummaterial (48) in dem flachen Graben aus n^+-Halbleitermaterial besteht.

5. Herstellungsverfahren für eine vertikale Transistor-/Kapazitätspeicherzellen-Halbleiterstruktur, nach Anspruch 1 bis 3, wobei
das Halbleitersubstrat (16) aus p^+-Halbleitermaterial besteht,
die Epitaxieschichten (14, 30, 32) aus p^--Halbleitermaterial bestehen,
das Polysilicium in dem tiefen Graben (26) und der epitaxiale Polysiliciumhals (34) aus p^+-Halbleitermaterial bestehen,
das Polysiliciummaterial (48) in dem flachen Graben aus p^+-Halbleitermaterial besteht.

6. Eine Speicherzellen-Halbleiterstruktur von einer Art, die einen vertikalen, selbstjustierend über einer Grabenspeicherkapazität angebrachten Zugriffstransistor einschließt, welche folgende Elemente umfaßt:
einen Halbleiterwafer, der ein Substrat (16) eines ersten Halbleitertyps und eine darauf angebrachte Epitaxieschicht (36) eines zweiten Halbleitertyps enthält,
einen in der Struktur aus Epitaxieschicht (36) und Substrat (16) angelegten tiefen Graben (26), wobei der tiefe Graben (26) eine zusammengesetzte isolierende Oxid/Nitridschicht (24) auf seinen vertikalen und horizontalen Oberflächen einschließt, um so eine Isolation für die Speicherkapazität zu erzeugen, und wobei der tiefe Graben (26) mit Polysilicium eines ersten Halbleitertyps gefüllt ist,
einen in der Epitaxieschicht (36) über dem Bereich des tiefen Grabens (26) angelegten flachen Graben (42), wobei der flache Graben eine auf seinen vertikalen und horizontalen Oberflächen aufgebrachte isolierende Oxidschicht (46) einschließt,
eine halsförmige Struktur (34) aus epitaxialem Polysiliciummaterial, die sich von der Oberfläche des mit Polysilicium gefüllten tiefen Grabens (26) hin zur darüberliegenden unteren Grenzfläche des flachen Grabens (42) erstreckt,
Störstellen, die in die Epitaxieschicht (36) zu beiden Seiten des darin liegenden flachen Grabens eingelagert werden, um Drain-HalbleiterÜbergänge (40) herzustellen,
und Polysiliciummaterial (48), das in dem flachen Graben (42) und über der Epitaxieschicht (36) angebracht wird, um Übertragungs-Halbleitergates bzw. Bereiche der Wortleitungen herzustellen.

7. Speicherzellen-Struktur nach Anspruch 6, worin
das Halbleitersubstrat (16) aus p^+-Halbleitermaterial besteht,
die Epitaxieschicht (36) aus p^--Halbleitermaterial besteht,
das Polysilicium in dem tiefen Graben (26) und der epitaxiale Polysiliciumhals (34) aus p^+-Halbleitermaterial bestehen,
das Polysiliciummaterial (48) in dem flachen Graben (42) aus n^+-Halbleitermaterial besteht.

3 comprend en outre les étapes suivantes :
- Etape 3A) La définition et l'implantation d'une région de puits de type n dans ladite troisième couche épitaxiale (32),
- Etape 3B) La formation d'une région de diffusion (40) dans ladite troisième couche épitaxiale de former une région de jonction de drain pour ladite cellule de mémoire.

4. Un procédé de fabrication d'une structure de cellule de mémoire à semiconducteur du type à condensateur de stockage - transistor d'accès vertical selon la revendication 1) à 3 dans lequel :
   - ledit substrat semiconducteur (16) est composé de matériau semiconducteur du type p+,
   - lesdites couches épitaxiales (14, 30, 32) sont composées de matériau semiconducteur du type p-,
   - ledit polysilicium dans ladite tranchée profonde (26) et ledit col de polysilicium épitaxial (34) sont composés de matériau semiconducteur du type p+, et
   - ledit polysilicium (48) dans ladite tranchée peu profonde est composé de matériau semiconducteur du type n+.

5. Un procédé de fabrication d'une structure de cellule de mémoire à semiconducteur du type à condensateur de stockage - transistor d'accès verticale selon les revendications 1 à 3 dans lequel :
   - ledit substrat semiconducteur (16) est composé de matériau semiconducteur du type p+,
   - lesdites couches supérieures (14, 30, 32) sont composées de matériau semiconducteur du type P-,
   - ledit polysilicium dans ladite tranchée profonde (26) et ledit col de polysilicium épitaxial (34) sont composés de matériau semiconducteur du type P+, et
   - ledit polysilicium (48) dans ladite tranchée peu profonde est composé de matériau semiconducteur du type p+.

6. Une structure de cellule de mémoire à semiconducteur du type comprenant un transistor d'accès vertical auto-aligné sur un condensateur de stockage en tranchée comprenant :
   - une microplaquette semiconductrice comprenant un substrat d'un premier type de semiconducteur (16) et une couche épitaxiale d'un second type de semiconducteur (36) disposée par dessus,
   - une tranchée profonde (26) ménagée dans ladite structure à couche épitaxiale (36) et substrat (16), ladite tranchée profonde (26) comprenant une couche d'isolation mixte d'oxyde-nitrure (24) sur ses surfaces verticales et horizontales pour assurer l'isolation du condensateur de stockage et dans laquelle ladite tranchée profonde (26) est remplie de polysilicium d'un premier type de semiconducteur,
   - une tranchée peu profonde (42) ménagée dans ladite couche épitaxiale (36) sur la région de ladite tranchée profonde (26), ladite tranchée peu profonde comprenant une couche d'isolation d'oxyde (46) sur ses surfaces verticales et horizontales,
   - une structure de col (34) de polysilicium épitaxiale s'étendant de la surface supérieure de ladite tranchée profonde remplie de polysilicium (26) à la surface inférieure de ladite tranchée peu profonde (42) ménagée par dessus,
   - des impuretés disposées dans ladite couche épitaxiale (36) de chaque côté de ladite tranchée peu profonde ménagée dans celle ci pour former des jonctions de drain de dispositif semiconducteur (40),
   - et du polysilicium (48) disposé dans ladite tranchée peu profonde (42) et sur ladite couche épitaxiale (36) pour former des régions de porte de transfert et de ligne de mots de dispositif semiconducteur, respectivement.

7. Une structure de cellule de mémoire selon la revendication 6 dans laquelle :
   - ledit substrat semiconducteur (16) est composé de matériau semiconducteur du type p+,
   - ledit couches épitaxiale (36) est composé de matériau semiconducteur du type p-,
   - ledit polysilicium dans ladite tranchée profonde (26) , et ledit col de polysilicium épitaxial (34) sont composés de matériau semiconducteur du type p+, et
   - ledit polysilicium (48) dans ladite tranchée peu profonde (42) est composé de matériau semiconducteur du type n+.

FIG. 3

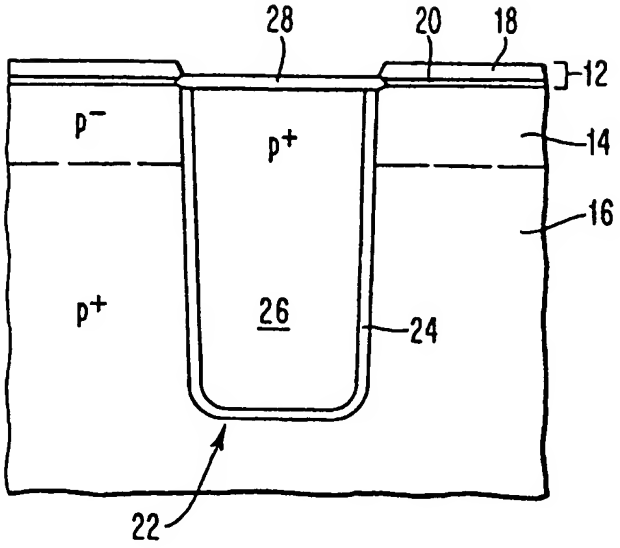


FIG. 4

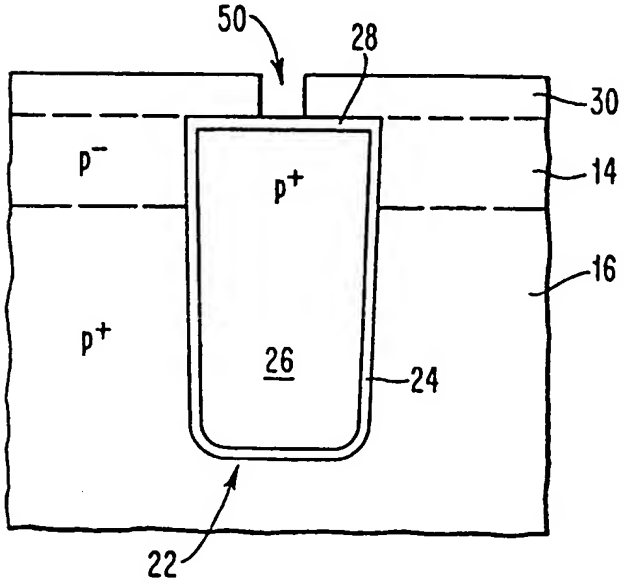


FIG. 7

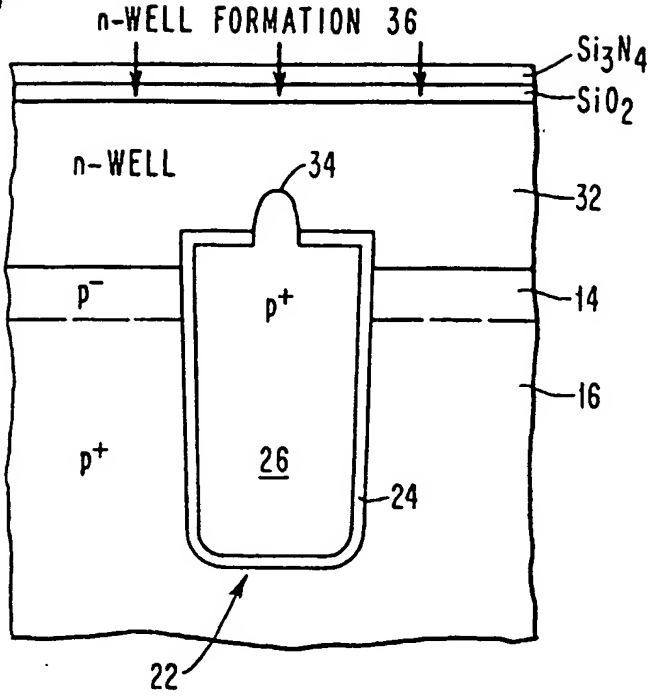
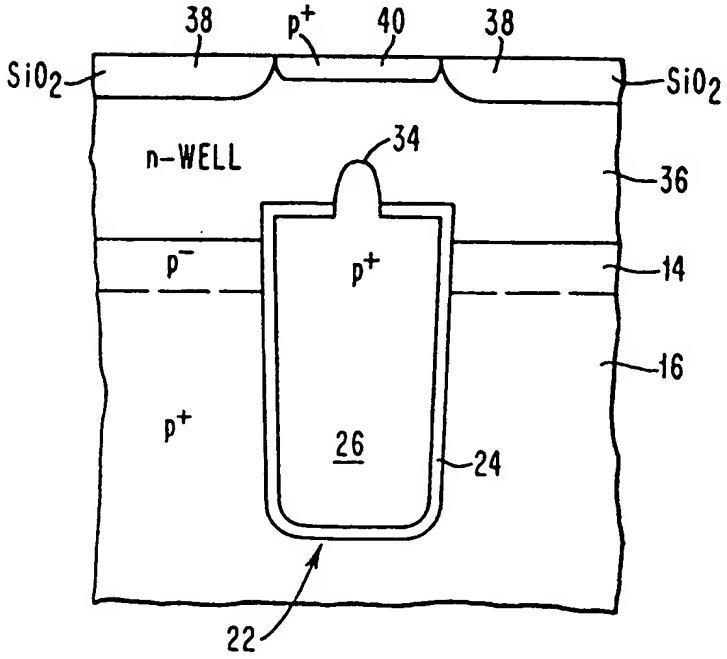

n-WELL FORMATION 36
Si_3N_4
SiO_2
n-WELL
34
32
p^-
p^+
14
16
p^+
26
24
22

FIG. 8


38
p^+
40
38
SiO_2
SiO_2
n-WELL
34
36
p^-
p^+
14
16
p^+
26
24
22